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Application No. 10/083,011 Attorney Docket No. PF010024
Customer No. 24498

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Edouard Ritz et al.
Application No.:	10/083,011
Filed:	February 25, 2002
Title:	Video Apparatus, Notably Video Decoder, and Process for Memory Control in such an Apparatus
Examiner:	Paulos M. Natnael
Art Unit:	2614

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioners for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May it please the Honorable Board:

This is Appellants' Brief on Appeal from the Final Rejection of Claims 1, 2 and 4-11. Please charge the fee for filing this brief to Deposit Account No. 07-0832. Appellants waive an oral hearing for this appeal.

Please charge any additional fee or credit overpayment to the above-indicated Deposit Account. Enclosed is a single copy of this Brief.

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Date: 6-19-06 Karen Scheunemann

I. Real Party in Interest

The real party in interest of Application Serial No. 10/083,011 is the Assignee of Record:

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II. Related Appeals and Interferences

There are currently, and have been, no related appeals or interferences regarding Application Serial No. 10/083,011, known to the undersigned attorney.

III. Status of the Claims

Claims 1, 2 and 4-11 have been rejected. The rejection of Claims 1, 2 and 4-11 is appealed. Claim 3 has been cancelled.

IV. Status of Amendments

No amendments were submitted subsequent to the Final Rejection. The rejected claims are included in the attached Appendix 1.

V. Summary of Claimed Subject Matter

Independent Claim 1 is directed to a video apparatus with a digital decoder (6) comprising a first memory (8) for storing video data, and a second memory (10) for storing on-screen display data. An on-screen

display circuit (12) generates an on-screen display graphics signal from the on-screen display data in the second memory (10). The first memory (8) is adapted to receive on-screen display data that is no longer being displayed, from the second memory (10), and to transfer said on-screen display data back to the second memory (10) in response to a request for display of data stored in the first memory (8).

Claim 2 is dependent from Claim 1 and adds the feature of a processing unit (14), the first memory (8) not being directly accessible by the processing unit (14).

Claim 4 is dependent from Claim 1 and adds the feature that the first memory (8) is a random access memory used for video decompression (page 3, lines 2 and 3).

Claim 5 is dependent from Claim 1 and adds the further feature that a digital decoder (6) is connected to a digital front end (4).

Claim 6 is directed to a process for controlling a video apparatus, comprising a digital decoder (6), a first memory (8), a second memory (10), and an on-screen display circuit (12) for generating an on-screen display signal based on data stored in the second memory (10), in which the method comprises the steps of writing on-screen display data to the second memory (10) for access by the on-screen display circuit (12), wherein the first memory is used for video decompression (page 3, lines 2 and 3), further comprising the steps of transferring on-screen display data that is no longer being displayed to the first memory (8), and upon request, transferring back on screen display data from the first memory (8) to the second memory (10).

Claim 7 is dependent from Claim 6 and sets forth the further steps of issuing a request for the on-screen display circuit (12) to use more than a given size in the second memory (10), and realizing a direct memory transfer of on-screen display data from the second memory (10) to the first memory (8).

Claim 8 is dependent from Claim 7 and sets forth the further steps of issuing a request for the on-screen display circuit (12) to use on-screen display data on the first memory (8) and transferring the on-screen display data to be used from the first memory (8) to the second memory (10).

Claim 9 is dependent from Claim 7 and adds the further feature that the transfer of on-screen display data to the first memory (8) occurs when the first memory (8) is unavailable for video decompression.

Claim 10 is dependent from Claim 1 and adds the further feature that transfer between the first (8) and second (10) memories is made using a direct memory access.

Claim 11 is dependent from Claim 4 and adds the feature that the first memory (8) is made available for storing on-screen display when the first memory (8) is not being used for holding video data.

VI. Grounds of Rejection to be Reviewed on Appeal

The Examiner has rejected Claims 4 and 6-11 under 35 U.S.C. 112 as failing to comply with the written description requirement.

The Examiner has rejected Claims 1, 2 and 4-11 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,263,396 to Cottle et al.

VII. Argument

Rejection of Claims 4 and 6-11 under 35 U.S.C. 112

The Examiner has asserted that in Claims 4 and 6, the recitation of "for video decompression" is new matter which was not described in the original specification. The attention of the Board is called to page 3, lines 2 and 3, of the instant specification, and to elements 6 and 8 of the instant drawing. The specification specifically states

"to decompress the MPEG stream, the MPEG decoder 6 is connected via a data bus to a video RAM 8".

Elements 6 and 8 are clearly shown in the Drawing. Furthermore, page 1, lines 10-12 of the instant specification recites that such a decoder circuit uses a so-called video RAM (random access memory) to retain data which are processed, for instance, to decompress an MPEG stream. It is therefore clear that the Examiner's rejection under 35 U.S.C. 112 is in error.

Rejection of Claims 1, 2 and 4-11 under 35 U.S.C. 103(a) over U.S. Patent 6,263,396 to Cottle et al.

In the instant invention, on-screen display circuit 12 receives data to be displayed from CPU RAM 10. In order to minimize the capacity of CPU RAM 10, so as to reduce its complexity and cost, the instant invention transfers OSD data which is not being used to video RAM 8. If CPU 14 calls for display of OSD data which is not in CPU RAM 10, the required data is transferred from video RAM 8 to CPU RAM 10.

Claim 1 specifically recites

"wherein the first memory (video RAM 8) is adapted to receive on-screen display data that is no longer being displayed from the second memory (CPU RAM 10) and to transfer said on-screen display data back to the second memory (CPU RAM 10) in response to a request for display of data stored in the first memory (video RAM 8)"

Nowhere do Cottle et al teach or suggest this structure. More specifically, nowhere do Cottle et al teach or suggest the transfer of OSD data between memories. Rather, Cottle et al teach transferring VBV buffer from SDRAM 312 to an operational memory on extension bus 300, in order to make room for OSD data. This is discussed in column 18, lines 33-40. Cottle et al also teach that OSD data may be stored in an external memory

attached to extension bus 300, as set forth in column 10, lines 21-23. However, nowhere do Cottle et al teach or suggest the transfer of OSD data between memories. Rather, Cottle et al teach that RAM 220 will turn on the OSD function, and specifies how and where OSD will be mixed and displayed, as explained in column 10, lines 22-26.

Nowhere do Cottle et al teach or suggest the transfer of OSD data from one memory to another, much less the transfer of OSD data that is no longer being displayed to a first memory which stores video data, as specifically recited in Claim 1. It is therefore clear that Cottle et al. utilize OSD data from whatever source holds such data, and that Cottle et al. do not transfer OSD data from one memory to another, as specifically recited in Claim 1.

The Examiner has asserted that it would be obvious to transfer OSD data between the memories of Cottle et al. The Appellants can not agree. Cottle et al. go to great lengths to make certain that sufficient memory is available to hold all of the OSD data. When such OSD data is needed for display, it is retrieved from whatever memory holds the OSD data which is required. Cottle et al. avoid transfer of OSD data between memories. It is therefore clear that Cottle et al teach away from transferring OSD data between memories. It is therefore clear that the Examiner's assertion that it would be obvious to transfer OSD data between the memories of Cottle et al. is in error, and that Claim 1 is patentable over Cottle et al under 35 USC 103.

Claims 2, 4, 5 and 10 are dependent from Claim 1 and contain further advantageous features. The Appellants submit that these subclaims are patentable as their parent Claim 1.

Claim 6 recites the method steps of

"transferring OSD data that is no longer being displayed to the first memory which is used for video decompression, and upon

request, transferring back OSD data from the first memory to the second memory"

Nowhere do Cottle et al show or suggest transfer of OSD data between memories, much less the transfer of OSD data that is no longer being displayed to a first memory which stores video data, as explained above. It is therefore clear that Cottle et al do not affect the patentability of Claim 6.

Merely because Cottle et al may store OSD data in multiple memories does not suggest the transfer of OSD data between memories. Cottle et al access OSD data from wherever it happens to reside. Nowhere do Cottle et al. teach or suggest the transfer of OSD data between memories, much less the transfer of OSD data that is no longer being displayed, from the second memory to the first memory, as specifically recited in Claim 6.

Furthermore, nowhere do Cottle et al show or suggest transferring OSD data that is no longer being displayed to the first memory, which is used for video decompression, as specifically recited in Claim 6.

The Examiner has asserted that it would be obvious to transfer OSD data between the memories of Cottle et al. The Appellants can not agree. As discussed above with regard to Claim 1, Cottle et al go to great lengths to make certain that sufficient memory is available to hold all of the OSD data. When such OSD data is needed for display, it is retrieved from whatever memory holds the OSD data which is required. Cottle et al avoid transfer of OSD data between memories. It is therefore clear that Cottle et al teach away from transferring OSD data between memories, and that the Examiner's assertion that it would be obvious to transfer OSD data between the memories of Cottle et al is in error.

Claims 7-9 are dependent from Claim 6 and add further advantageous features. The Appellants submit that these subclaims are patentable as their parent Claim 6.

It is therefore clear that the Examiner's rejection. is in error, and that the rejection should be reversed.

Respectfully submitted,

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Appendix I

Claims on Appeal

1. A video apparatus with a digital decoder comprising:

a first memory for storing video data;

a second memory for storing on-screen display data;

an on-screen display circuit for generating on-screen display graphics signal from the on-screen display data in the second memory;

wherein the first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and to transfer said on-screen display data back to the second memory in response to a request for display of data stored in the first memory.

2. A video apparatus according to claim 1, further comprising a processing unit, the first memory not being directly accessible by the processing unit.

4. A video apparatus according to claim 1, wherein the first memory is a random access memory used for video decompression.

5. A video apparatus according to claim 1, wherein the digital decoder is connected to a digital front-end.

6. A process for controlling a video apparatus comprising a digital decoder, a first memory, a second memory and an on-screen display circuit for generating an on-screen display signal based on data stored in the second memory, said method comprising the steps of:

writing on-screen display data to the second memory for access by the on-screen display circuit;

wherein, the first memory is used for video decompression, further comprising the steps of:

transferring on-screen display data that is no longer being be displayed to the first memory; and

upon request, transferring back on-screen display data from the first memory to the second memory.

7 A process according to claim 6, further comprising the steps of:

- issuing a request for the on-screen display circuit to use more than a given size in the second memory,
- realizing a direct memory transfer of on-screen display data from the second memory to the first memory.

8. A process according to claim 7, further comprising the steps of:

- issuing a request for the on-screen display circuit to use on-screen display data in the first memory, and
- transferring said on-screen display data to be used from the first memory to the second memory.

9. A process according to claim 7, wherein the transfer of on-screen display data to the first memory occurs when the first memory is unavailable for video decompression.

10. A video apparatus according to claim 1, wherein transfer between the first and second memories is made using a direct memory access.

11. A video apparatus according to claim 4, wherein the first memory is made available for storing on-screen display where the first memory is not being used for holding video data.